PATENT
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	)	
Hong Sung SONG	)	Confirmation No. 8778
Application No.: 10/021,009	)	Group Art Unit: 2675
Filed: December 19, 2001	)	Examiner: A. Awad
For: METHOD AND APPARATUS FOR DRIVING A LIQUID CRYSTAL DISPLAY PANEL IN A DOT INVERSION SYSTEM	)	**Mail Stop Appeal Brief - Patents**

Commissioner for Patents
U.S. Patent and Trademark Office
Mail Stop Appeal Brief - Patents
Alexandria, VA 22314

APPELLANT'S BRIEF UNDER 37 C.F.R. § 41.31

This brief is in furtherance of the Notice of Appeal, filed in the above-identified patent application on February 15, 2005. The fee set forth under 37 C.F.R. § 41.20(b)(2) is being filed concurrently herewith.

1. The Real Party In Interest

The real party in interest in this appeal is LG.Philips LCD Co, Ltd. of Seoul, Korea.

2. Related Appeals and Interferences

Appellant is not aware of any other appeals or interferences that will directly affect, or be directly affected by, or have a bearing on the Board's decision in the appeal.

3. Status of Claims

The status of the claims is as follows:

Claims rejected: 1-13.
Claims objected to: 1, 5, and 10.
Claims allowed: none.
Claims withdrawn: none.
Claims canceled: none.
Claims appealed: 1-13.

4. Status of Amendments

No Amendments have been filed subsequent to the Final Office Action dated August 17, 2004. Accordingly, pending/originally-filed claims are attached as Appendix A to this brief.

5. Summary of the Claimed Subject Matter

An aspect of Appellant's present invention relates generally to a method of driving a liquid crystal display panel, a driving apparatus for a liquid crystal display panel, and a device for driving a liquid crystal display panel.

Independent Claim 1

With respect to independent claim 1, as discussed in Appellant's specification beginning at paragraph [0033] at page 10 and shown in FIGs. 6-10, a method of driving a liquid crystal display panel 10 of a dot inversion system having liquid crystal cells arranged at intersections between a plurality of data lines DL1, DL2, DL3,...DLn-2, DLn-1, DLn and a plurality of gate lines GL1, GL2, GL3,...GLm-2, GLm-1, GLm in a matrix array includes steps of supplying the data lines DL1, DL2, DL3,...DLn-2, DLn-1, DLn with $(n-2)^{th}$ data

corresponding to the liquid crystal cells connected to an $(m-2)^{th}$ gate line, wherein m and n are integers both greater than or equal to 2, conducting a first data supplying channel for the liquid crystal cells connected to the m^{th} gate line such that the $(n-2)^{th}$ data is supplied to the liquid crystal cells connected to the m^{th} gate line, and conducting a second data supplying channel for the liquid crystal cells connected to the $(m-2)^{th}$ gate line such that the $(n-2)^{th}$ data is supplied to the liquid crystal cells connected to the $(m-2)^{th}$ gate line, wherein conducting the first data supplying channel and conducting the second data supplying channel are performed simultaneously.

Independent Claim 5

With regard to independent claim 5, a driving apparatus for a liquid crystal display panel 10 of dot inversion system having liquid crystal cells arranged at intersections between a plurality of data lines DL1, DL2, DL3,...DLn-2, DLn-1, DLn and a plurality of gate lines GL1, GL2, GL3,...GLm-2, GLm-1, GLm in a matrix array includes a data driving integrated circuit 8 supplying data to the data lines DL1, DL2, DL3,...DLn-2, DLn-1, DLn of the liquid crystal display panel 10, a gate driving integrated circuit 9 responding to a gate start pulse GSP to sequentially drive the gate lines GL1, GL2, GL3,...GLm-2, GLm-1, GLm of the liquid crystal display panel 10, and a pre-charging controller 11 continuously generating first and second gate start pulses such that data corresponding to an $(n-2)^{th}$ data line is supplied to an n^{th} data line, wherein n is an integer greater than or equal to 2, and applying the first and second gate start pulses to the gate driving integrated circuit 9.

Independent Claim 10

With regard to independent claim 10, a device for driving a liquid crystal display panel 10 having a plurality of data lines DL1, DL2, DL3,...DLn-2, DLn-1, DLn, a plurality of gate lines GL1, GL2, GL3,...GLm-2, GLm-1, GLm orthogonal to the plurality of data lines DL1, DL2, DL3,...DLn-2, DLn-1, DLn, and a plurality of liquid crystal cells includes a data driving 8 integrated circuit supplying data to the data lines DL1, DL2, DL3,...DLn-2, DLn-1, DLn, a gate driving integrated circuit 9 responding to a gate start pulse GSP to drive the gate lines GL1, GL2, GL3,...GLm-2, GLm-1, GLm, and a pre-charging controller 11 generating first and second gate start pulses to the gate driving integrated circuit 9, wherein data corresponding to an $(n-2)^{th}$ data line is supplied to an n^{th} data line, wherein n is an integer greater than or equal to 2.

6. Grounds of Rejection To Be Reviewed On Appeal

Claims 1-13 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Miyahara et al. (US 6,075,507) in view of Asada et al. (US 5,867,141).

7. Argument

(i) Rejections under 35 U.S.C. § 112, first paragraph

No claims are presently rejected under 35 U.S.C. § 112, first paragraph.

(ii) Rejections under 35 U.S.C. § 112, second paragraph

No claims are presently rejected under 35 U.S.C. § 112, second paragraph.

(iii) Rejections under 35 U.S.C. § 102

No claims are presently rejected under 35 U.S.C. § 102.

(iv) Rejections under 35 U.S.C. § 103

Claims 1-13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Miyahara et al. (US 6,075,507) in view of Asada et al. (US 5,867,141). Appellant respectfully traverses this rejection as being based upon a reference that neither teaches nor suggests the novel combination of features recited in independent claims 1, 5, and 10, and hence dependent claims 2-4, 5-9, and 11-13.

The Office Action admits that "Miyahara does not expressly teach conducting the data supply channel and conducting the data-supplying channel are performed simultaneously." Thus, the Office Action relies upon Asada et al. for allegedly teaching "a driving method for liquid crystal display wherein the data supply channel and data-supplying channel are performed simultaneously (col. 13, lines 31-38)." As a result, the Office Action concludes that "[i]t would have been obvious to a person of ordinary skill in the art at the time the invention was made to include the teaching of Asada for simultaneously applying data to be incorporated to Miyahara's device so as motivated by Asada, to be able to permit a competent image quality to be secured with a stable high contrast (col. 3, lines 62-65)." Appellant respectfully disagrees.

Appellant respectfully submits that Asada et al. fails to provide proper motivation with which to modify Miyahara et al. since Asada et al. fails to teach or suggest the desirability of simultaneously "conducting the first data supplying channel and conducting the second data supplying channel." The specific passage cited by the Office Action of Asada et al. clearly fails to support the Office Action's allegation that "the data supply channel and data-supplying channel are performed simultaneously." Claim 6 of Asada et al.

provides no motivation whatsoever to modify Miyahara et al. "to be able to permit a competent image quality to be secured with a stable high contrast." Asada et al. discloses (col. 3, lines 62-65) that a gate storage structure "having a high opening ratio" permits a competent image quality to be secured with a stable high contrast, and nothing with regards to simultaneously supplying data.

Furthermore, the Office Action alleges (see Response to Arguments #5 of Final Office dated August 17, 2004) that "Asada made it clear that by simultaneously supplying data, high contrast will be achieved (col. 1, lines 65-67)." However, Asada et al. discloses *absolutely nothing* with regard to "high contrast" at col. 1, lines 65-67. Thus, Appellant respectfully asserts that the Office Action again has completely failed to provide any proper motivation to modify Miyahara et al. to arrive at Applicant's claimed invention.

MPEP § 2143.01 instructs that "[t]he mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggest the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990)." Accordingly, because the applied art is completely silent and does not suggest any desirability of the Office Action's alleged combination, Appellant respectfully asserts that the Office Action has clearly not established any type of *prima facie* case of obviousness.

Regarding independent claims 5 and 10, Appellant respectfully asserts that Asada et al. fails to teach or suggest "a pre-charging controller continuously generating first and second gate start pulses such that data corresponding to an $(n-2)^{th}$ data line is supplied to an n^{th} data line, wherein n is an integer greater than or equal to 2" and "applying the first and second gate start pulses to the gate driving integrated circuit." In addition, Appellant respectfully asserts that the Office Action's allegation that the claimed pre-charging

controller is "fairly similar to the blanking period shown in figure 5 of Asada's device" and that "the claims are substantially similar to claims 5 and 7-9 respectively, and would be analyzed as previously discussed with respect to claims 5 and 7-9 above" is simply not correct and wholly untrue. For example, the blanking period shown in FIG. 5 of Asada et al. fails to even begin to disclose "continuously generating first and second gate start pulses such that data corresponding to an $(n-2)^{th}$ data line is supplied to an nth data line, wherein n is an integer greater than or equal to 2," as recited by independent claims 5 and 10, and "applying the first and second gate start pulses to the gate driving integrated circuit," as recited by independent claim 5.

For at least the above reasons, Appellant asserts that claims 1-13 are neither taught nor suggested by the applied prior art references, whether taken alone or in combination. Thus, Appellant respectfully asserts that the rejection under 35 U.S.C. §103(a) should be withdrawn because the above-discussed novel combination of features are neither taught nor suggested by any of the applied references.

(v) Other Rejections

No claims are presently rejected under grounds other than those referred to above.

In view of the foregoing, Appellant respectfully requests the reversal of the Examiner's rejection and allowance of the pending claims. If there are any other fees due in connection with the filing of this Appeal Brief, please charge the fees to our Deposit Account No. 50-0310.

If a fee is required for an extension of time under 37 C.F.R. §1.136 not accounted for above, such an extension is requested and the fee should also be charged to our Deposit Account No. 50-0310.

Respectfully submitted,

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8. Claims Appendix

Claim 1 (Previously Presented): A method of driving a liquid crystal display panel of a dot inversion system having liquid crystal cells arranged at intersections between a plurality of data lines and a plurality of gate lines in a matrix array, comprising the steps of:

supplying the data lines with (n-2)th data corresponding to the liquid crystal cells connected to an (m-2)th gate line, wherein m and n are integers both greater than or equal to 2;

conducting a first data supplying channel for the liquid crystal cells connected to the mth gate line such that the (n-2)th data is supplied to the liquid crystal cells connected to the mth gate line; and

conducting a second data supplying channel for the liquid crystal cells connected to the (m-2)th gate line such that the (n-2)th data is supplied to the liquid crystal cells connected to the (m-2)th gate line,

wherein conducting the first data supplying channel and conducting the second data supplying channel are performed simultaneously.

Claim 2 (Original): The method according to claim 1, wherein the liquid crystal cells connected to first and second gate lines of the plurality of gate lines are charged at every frame with data signals applied at a blanking interval.

Claim 3 (Original): The method according to claim 2, wherein polarity inversion of the data signals applied to the liquid crystal cells connected to the first and second gate lines is made in at least two clock time intervals prior to an application of an active data signal.

Claim 4 (Original): The method according to claim 2, wherein gate and data control signals for applying data to the liquid crystal cells connected to the first and second gate lines are applied in at least two clock time intervals before the gate and data control signals become effective data.

Claim 5 (Previously Presented): A driving apparatus for a liquid crystal display panel of dot inversion system having liquid crystal cells arranged at intersections between a plurality of data lines and a plurality of gate lines in a matrix array, comprising:

a data driving integrated circuit supplying data to the data lines of the liquid crystal display panel;

a gate driving integrated circuit responding to a gate start pulse to sequentially drive the gate lines of the liquid crystal display panel; and

a pre-charging controller continuously generating first and second gate start pulses such that data corresponding to an (n-2)th data line is supplied to an nth data line, wherein n is an integer greater than or equal to 2, and applying the first and second gate start pulses to the gate driving integrated circuit.

Claim 6 (Original): The apparatus according to claim 5, wherein the pre-charging controller includes:

a first input line supplied with a pre-gate start pulse and a second input line supplied with a data enable signal for controlling data output of the data driving integrated circuit;

first delay means for delaying the pre-gate start pulse from the first input line by one clock interval of the data enable signal;

second delay means for delaying the delayed pre-gate start pulse from the first delay means by one clock interval of the data enable signal; and

a gate device for executing an exclusive logical sum operation of the pre-gate start pulse from the first input line and an output signal of the second delay means to continuously output the first and second gate start pulses.

Claim 7 (Original): The apparatus according to claim 5, wherein the liquid crystal cells connected to the first and second gate lines of the liquid crystal display panel are charged at every frame interval with data signals applied at a blanking interval.

Claim 8 (Original): The apparatus according to claim 7, wherein polarity inversion of the data signals applied to the liquid crystal cells connected to the first and second gate lines is made in at least two clock time intervals prior to an application of an active data signal.

Claim 9 (Original): The apparatus according to claim 7, wherein gate and data control signals for applying data to the liquid crystal cells connected to the first and second gate lines are applied in at least two clock time intervals before the gate and data control signals become effective data.

Claim 10 (Previously Presented): A device for driving a liquid crystal display panel having a plurality of data lines, a plurality of gate lines orthogonal to the plurality of data lines, and a plurality of liquid crystal cells, comprising:

a data driving integrated circuit supplying data to the data lines;

a gate driving integrated circuit responding to a gate start pulse to drive the gate lines; and

a pre-charging controller generating first and second gate start pulses to the gate driving integrated circuit, wherein data corresponding to an (n-2)th data line is supplied to an nth data line, wherein n is an integer greater than or equal to 2.

Claim 11 (Original): The device according to claim 10, wherein the liquid crystal cells connected to the first and second gate lines of the liquid crystal display panel are charged at every frame interval with data signals applied at a blanking interval.

Claim 12 (Original): The apparatus according to claim 10, wherein polarity inversion of the data signals applied to the liquid crystal cells connected to the first and second gate lines is made in at least two clock time intervals prior to an application of an active data signal.

Claim 13 (Original): The apparatus according to claim 10, wherein gate and data control signals for applying data to the liquid crystal cells connected to the first and second gate lines are applied in at least two clock time intervals before the gate and data control signals become effective data.

9. Evidence Appendix

No information is appended under this section.

10. Related Proceedings Appendix

No information is appended under this section.